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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,401	06/23/2003	Zoran Krivokapic	H1938	7785

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THE CAVANAGH LAW FIRM
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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,401	KRIVOKAPIC, ZORAN	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-23* is/are rejected.

7)☒ Claim(s) *18 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 9/13/04. Currently, claims 1-24 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 9/02/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is indefinite whether the "protecting the silicide of the second layer", in claim 24, is the "second layer of semiconductor material" or the "second layer of the dielectric material". For

examination purposes on the merits, the Examiner, will assume the "second layer of semiconductor material".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11, 13-16, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwamatsu et al., US Patent 5,905,286.

Iwamatsu discloses the semiconductor method as claimed. See figures 1-219, with emphasis on figures 1-23, 126-129, and 141-145, and corresponding text, where Iwamatsu teaches a method of manufacturing a semiconductor device, comprising: providing a semiconductor substrate **1** (figure 1; col. 17, lines 19-27); forming a mesa structure from the semiconductor substrate, wherein the mesa structure has a first surface and first and second sidewalls (figures 8-11; col. 18, lines 1-18; col. 19, lines 17-63); forming a gate structure over the mesa structure (figure 14 and 15; col. 19, lines 59-67), wherein the gate structure has a gate surface and first and second sides, and wherein first and second portions of the gate structure are disposed on the first and second sidewalls, respectively (figures 14-17; col. 17, lines 28-41; col. 19, lines 59-67); and doping portions of the semiconductor substrate adjacent the first and second sides of the gate structure (figures 13-17; col. 17, lines 28-41).

Pertaining to claim 2, Iwamatsu teaches, the method wherein forming the gate structure includes forming a first layer of dielectric material **12** over the mesa structure (figures 8-11; col. 19, lines 1-44).

Pertaining to claim 3, Iwamatsu teaches, the method wherein forming the gate structure includes forming a second layer of dielectric material over the first layer of dielectric material (figure 18; col. 20, lines 19-24).

Pertaining to claim 4, Iwamatsu teaches the method wherein forming the first layer of dielectric material includes forming portions of the first layer of dielectric material over the first and second sidewalls, and wherein a portion of the first layer of dielectric material serves as the first portion of the gate structure and another portion of the first layer of dielectric material serves as the second portion of the gate structure (figure 14; col. 19, lines 59-67).

Pertaining to claim 5, Iwamatsu teaches the method wherein forming portions of the first layer of dielectric material over the first and second sidewalls includes oxidizing the first and second sidewalls (figures 8-11; col. 19, lines 1-44).

Pertaining to claim 6, Iwamatsu teaches the method further including forming a layer of semiconductor material over the semiconductor substrate adjacent the first and second sides of the gate structure (col. 17, lines 20-41).

Pertaining to claim 7, Iwamatsu teaches the method wherein forming the layer of semiconductor material includes selectively growing the layer of semiconductor material (figure 126; col. 33, lines 40-51).

Pertaining to claim 8, Iwamatsu teaches the method wherein selectively growing includes selectively growing a semiconductor material selected from the group of semiconductor

materials consisting of silicon, silicon germanium, and germanium (figure 126; col. 33, lines 40-51).

Pertaining to claim 9, Iwamatsu teaches the method wherein doping the semiconductor substrate comprises: implanting a dopant into the layer of semiconductor material adjacent the first and second sides of the gate structure using an angled implant (col. 20, lines 8-44); and implanting additional dopant into the layer of semiconductor material adjacent the first and second sides of the gate structure using zero degree implant (figure 17; col. 19, lines 45-67; col. 20, lines 1-44) .

Pertaining to claim 10, Iwamatsu teaches the method further including forming silicide from the layer of semiconductor material (col. 20, lines 19-44).

Pertaining to claim 11, Iwamatsu teaches the method further including forming silicide from the gate structure (col. 20, lines 25-55).

Pertaining to claim 13, Iwamatsu teaches the method wherein providing the semiconductor substrate includes providing a semiconductor-on-insulator semiconductor substrate (col. 17, lines 20-42).

Pertaining to claim 14, Iwamatsu teaches the method for manufacturing a strained semiconductor device suitable for use in an integrated circuit, comprising: providing a semiconductor-on-insulator mesa isolation structure, the semiconductor–on-insulator mesa structure having a top surface and first and second sidewalls (figure 1; col. 17, lines 19-27); forming a gate dielectric material on the to surface and the first and second sidewalls (figures 14-15; col. 19, lines 59-67); forming a gate on the gate dielectric material, wherein the gate and the gate dielectric material cooperate to form a gate structure having a top surface and gate sidewalls

(figures 14-16; col. 19, lines 59-67; col. 20, lines 1-8); forming a semiconductor material on portions of the top surface of the mesa isolation structure adjacent to the first and second sidewalls (figure 11; col. 19, lines 35-44); forming a silicide from the semiconductor material (figures 20 and 21;col. 20, lines 25-55); and forming silicide from the gate, wherein the silicide from the gate strains the semiconductor device (figures 20 and 21; col. 20, lines 25-55).

Pertaining to claim 15, Iwamatsu teaches the method wherein providing the semiconductor-on-insulator mesa isolation structure includes forming portions of the first and second sidewalls to be below the top surface of the semiconductor-on-insulator mesa isolation structure (figure 11; col. 19, lines 40-44).

Pertaining to claim 16, Iwamatsu teaches the method wherein forming the gate dielectric material includes oxidizing the portions of the first and second sidewalls below the top surface of the semiconductor-on-insulator structure (col. 19, lines 59-67).

Pertaining to claim 19, Iwamatsu teaches a method for straining a semiconductor device, comprising: providing a semiconductor substrate comprising a first layer of semiconductor material disposed over a layer of dielectric material, the semiconductor substrate having a top surface and isolation sidewalls (figure 11; col. 19, lines 40-44); forming a gate structure on the semiconductor substrate, the gate structure having a gate surface, first and second opposing gate sidewalls, and third and fourth opposing gate sidewalls (figure 19); and forming silicide from the gate surface and the first and second opposing gate sidewalls of the gate structure, wherein the silicide strains the semiconductor material of the semiconductor substrate (figures 20-23).

Pertaining to claim 20, Iwamatsu teaches the method further including forming a second layer of semiconductor material on the portions of the first layer of semiconductor material adjacent the third and fourth opposing gate sidewalls (figure 139; col. 35, lines 37-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12, 17, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamatsu et al., US Patent 5,905,286 in view of Chen et al. Patent Application Publication 2004/0197969.

Iwamatsu discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1-11, 13-16, and 19 under 35 U.S.C. 102(b).

However, Iwamatsu fails to show, pertaining to claims 12 and 17, the method wherein forming silicon from the layer of semiconductor material and from the gate structure includes forming nickel silicide. In addition, Iwamatsu fails to show, pertaining to claim 21, the method further including protecting the gate structure before forming the second layer of semiconductor material. Also, Iwamatsu fails to show, pertaining to claim 22, the method further including doping the second layer of semiconductor material. Iwamatsu fails to show, pertaining to claim 23, the method further including forming silicide from the second layer of semiconductor material. Finally, Iwamatsu fails to show, pertaining to claim 24, the method further including

protecting the silicide from the second layer of dielectric material before forming the silicide from the gate surface.

Chen teaches, on figures 1a-5b, and corresponding text, a similar method of manufacturing a strained semiconductor device, where a second semiconductor layer is formed by selective epitaxial growth and doped with impurities. In addition, Chen teaches protecting the gate structure before forming the second layer of semiconductor material. Also, Chen teaches forming a silicide on the second layer of semiconductor material (paragraph [0035] and [0039-0043].

It would have been obvious to one of ordinary skill in the art to substitute, pertaining to claims 12 and 17, the method wherein forming silicon from the layer of semiconductor material and from the gate structure includes forming nickel silicide. In addition, it would have been obvious, pertaining to claim 21, to substitute the method further including protecting the gate structure before forming the second layer of semiconductor material. Also, it would have been obvious, pertaining to claim 22, to substitute, the method further including doping the second layer of semiconductor material. It would have been obvious, pertaining to claim 23, to substitute, the method further including forming silicide from the second layer of semiconductor material, in the method of Iwamatsu, according to the teachings of Chen, with the motivation that, silicides produce lower electrical resistance. Therefore, it would be more desirable to one of ordinary skill in the art to use a nickel silicide, for the purpose forming a contact with lower electrical resistance, resulting in a more reliable semiconductor device. The gate structure, taught in Chen, has protective sidewalls formed on sides of the gate electrode, and the raised source/drain regions formed by conventional selective epitaxy are then doped. Therefore, it

would be obvious that one of ordinary skill in the art would protect the gate structure before forming the second layer of semiconductor and subsequently doping the semiconductor material, for the purpose of protecting the gate structure while creating source drain regions within the semiconductor device.

Allowable Subject Matter

Claims 18 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The closes prior art of record, fails to show, pertaining to claim 18, forming the semiconductor material on portions of the top surface of the mesa isolation structure includes forming a protective material over the gate before forming the semiconductor material. In addition, the closest prior art of record, fails to show, pertaining to claim 24, (assuming the "semiconductor material") protecting the silicide formed from the second layer of semiconductor material before forming the silicide from the gate surface.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
November 20, 2004

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